What is claimed is:

1. A semiconductor device comprising:

a memory chip including bonding pads which are arranged along a first side corresponding to address terminals and bonding pads which are arranged along a second side which faces the first side in an opposed manner corresponding to data terminals;

a package substrate including bonding leads which are formed corresponding to the first side of the memory chip, bonding leads which are formed corresponding to the second side of the memory chip, and address terminals and data terminals which are connected to the bonding leads;

a semiconductor chip which includes an address output circuit and a data input/output circuit which are also served for memory access and a signal processing circuit having a data processing function, wherein bonding pads which are connected to the bonding leads of the package substrate corresponding to the address terminals and bonding pads which are connected to the bonding leads of the package substrate corresponding to the data terminals are arranged so as to be distributed to two sides out of four sides,

wherein the memory chip and the semiconductor chip are mounted on the package substrate in a stacked structure.

2. A semiconductor device according to claim 1, wherein the corresponding terminals of the semiconductor chip and the memory chip are connected to each other by wires with respect

to the bonding leads which are formed in common on the package substrate.

3. A semiconductor device according to claim 1,

wherein in conformity with pitches of respective bonding pads of address and data of the memory chip, the respective bonding pads of the corresponding address and data of the semiconductor chip are arranged, and

wherein between the respective bonding pads for address and data of the semiconductor chip, bonding pads which are independently formed on the semiconductor chip so as to conform to the memory-chip side pitch are suitably arranged.

4. A semiconductor device according to claim 1, wherein the package substrate forms wiring layers respectively on a front surface on which the semiconductor chip is mounted and on a back surface on which balls constituting external terminals are formed, and corresponding wiring layers are connected by through holes.

5. A semiconductor device according to claim 4,

wherein the semiconductor chip constitutes a one chip microcomputer, and

wherein bonding pads which are connected to external terminals necessary for the microcomputer are also arranged on remaining two sides out of four sides.

6. A semiconductor device according to claim 5,

wherein the memory chip has an area larger than an area of the semiconductor chip and is formed into a rectangular shape in which a length of the first side and the second side is shorter

than a length of other two sides, and

wherein with respect to rows of the bonding leads which are formed corresponding to the first side and the second side of the memory chip, the pull-out directions of wiring layers leading to the through holes are arranged to extend toward the inside of the package substrate.

7. A semiconductor device according to claim 6,

wherein the memory chip is mounted on the surface of the package substrate, and

wherein the semiconductor chip is mounted on a surface of the memory chip so as to provide a stacked structure.

8. A semiconductor device according to claim 5, wherein with respect to the rows of bonding leads which are formed corresponding to two sides other than the first side and second side of the memory chip, the pull-out directions of the wiring layers leading to the through holes are distributed to the inside and the outside of the package substrate.

9. A semiconductor device according to claim 8, wherein with respect to a length of the bonding leads which are formed corresponding to the first side and the second side of the memory chip, a length of the bonding leads which are formed corresponding to two sides other than the first side and the second side of the memory chip is made short.

10. A semiconductor device according to claim 6, wherein the bonding leads of the package substrate corresponding to the first side and the second side of the memory chip are formed into a rectangular shape such that the longitudinal direction

thereof is directed in the extension direction of wires which perform the connection of the bonding leads with the bonding pads of the corresponding memory chip and the semiconductor chip corresponding to the bonding leads.

11. A semiconductor device according to claim 7, wherein the bonding leads which are respectively formed corresponding to the first side and the second side of the memory chip are bonding leads having portions thereof over which wires connected to other bonding leads pass notched.

12. A semiconductor device according to claim 10,

wherein the bonding leads which are respectively formed corresponding to the first side and the second side of the memory chip are arranged in a staggered manner in two inner and outer rows along the extension direction of wires which are connected to the bonding leads, and

wherein notched portions are formed on inner ends of the inside bonding leads.

13. A semiconductor device comprising:

a semiconductor chip which includes bonding pads arranged along at least a first side and a second side which faces the first side in an opposed manner; and

a package substrate which includes bonding leads formed corresponding to the first side and the second side of the semiconductor chip and external terminals connected to the bonding leads,

wherein the bonding leads have portions thereof over which wires connected to other bonding leads pass notched.

14. A semiconductor device comprising:

a semiconductor chip including bonding pads which are arranged along at least a first side and a second side which faces the first side in an opposed manner; and

a package substrate including bonding leads which are formed corresponding to the first side and the second side of the semiconductor chip and external terminals which are connected to the bonding leads,

wherein the bonding leads are arranged in a staggered manner at two inner and outer rows along the extension direction of wires which are connected to the bonding leads,

wherein the pull-out direction of wiring layers leading to respective lead through holes are directed toward the inside of the package substrate, and

wherein notched portions are formed in inner ends of the inside bonding leads.